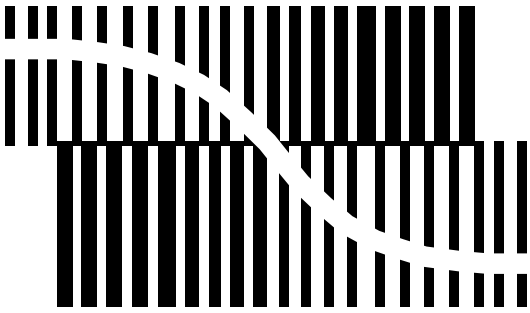
DATA SHEET



BITSTREAM CONVERSION

SAA7360
Bitstream conversion ADC for digital audio systems

Product specification
Supersedes data of July 1993
File under Integrated Circuits, IC01

1995 Apr 24

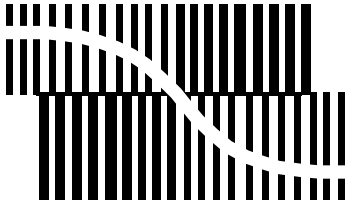
PHILIPS

Bitstream conversion ADC for digital audio systems

SAA7360

FEATURES

- Stereo input
- Single-ended input
- Uncommitted input buffer for filtering and pre-scaling
- Fully differential analog-to-digital converter (ADC) using 3rd order Sigma-Delta modulation
- 128 times oversampling
- Four stage digital decimation filter
- Switchable high-pass filter to remove DC offsets
- 16-bit or 18-bit selectable output in a multiple of formats
- Sampling rates between 18 and 53 kHz supported
- Master or slave operation
- Choice of 2 crystal frequencies
- Single power supply operation (+5 V).



GENERAL DESCRIPTION

The SAA7360 is a CMOS ADC using Philips bitstream conversion technique. The device is designed for digital audio playback systems, such as digital amplifiers, CD-recordable and Digital Compact Cassette (DCC). The device is a complementary device to the SAA7350 bitstream conversion digital-to-analog converter (DAC).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.5	5.0	5.5	V
f_{xtal}	crystal frequency	$256f_s$	–	11.2896	–	MHz
		$512f_s$	–	22.5792	–	MHz
THD + N	total harmonic distortion + noise		–	–90	–85	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7360GP	QFP44[1]	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

Note

1. When using IR reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Pocketbook"* (order number 9398 510 34011) are followed.

BLOCK DIAGRAM

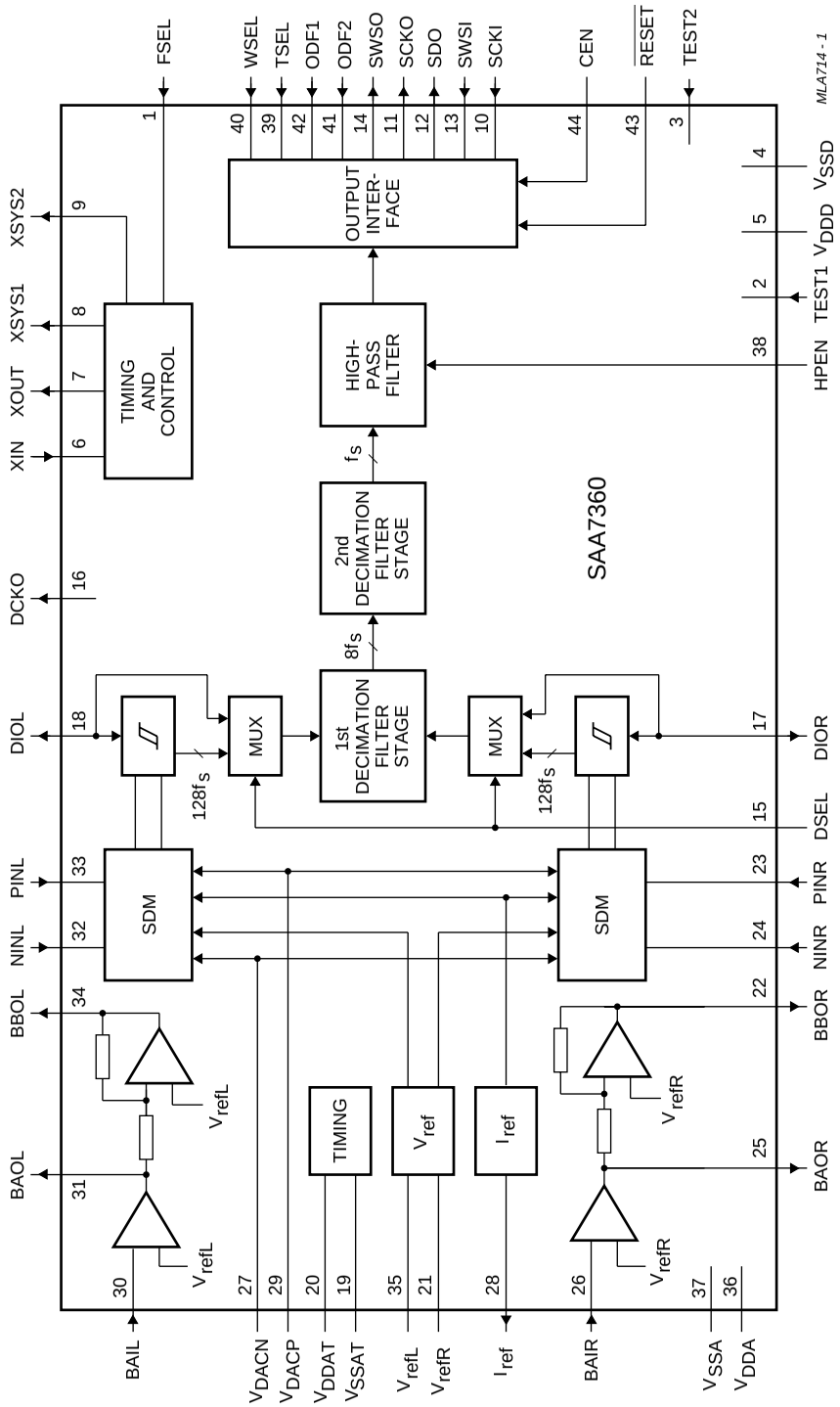


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSEL	1	Crystal frequency select input. This pin is used to select the master crystal frequency as follows: FSEL = HIGH = $256f_s$; FSEL = LOW = $512f_s$; if unconnected the pin will default HIGH.
TEST1	2	test input 1; this pin should be left open-circuit
TEST2	3	test input 2; this pin should be left open-circuit
V_{SSD}	4	supply ground for the digital section
V_{DDD}	5	supply voltage for the digital section (+5 V)
XIN	6	crystal oscillator input
XOUT	7	crystal oscillator output
XSYS1	8	system clock output
XSYS2	9	output clock at a frequency half the system clock frequency
SCKI	10	serial interface clock input
SCKO	11	serial interface clock output
SDO	12	serial interface data output
SWSI	13	serial interface word select input
SWSO	14	serial interface word select output
DSEL	15	input for selecting between the internally generated 1-bit code (DSEL = HIGH) or an externally generated 1-bit code (DSEL = LOW); if unconnected this pin defaults HIGH
DCKO	16	1-bit code clock output
DIOR	17	1-bit code input/output (right channel)
DIOL	18	1-bit code input/output (left channel)
V_{SSAT}	19	supply ground for the analog timing section
V_{DDAT}	20	supply voltage for the analog timing section (+5 V)
V_{refR}	21	voltage reference generator for the right channel analog section
BBOR	22	output of right channel buffer operational amplifier ‘B’
PINR	23	positive input to right channel Sigma-Delta modulator
NINR	24	negative input to right channel Sigma-Delta modulator
BAOR	25	output of right channel buffer operational amplifier ‘A’
BAIR	26	input of right channel buffer operational amplifier ‘A’
V_{DACN}	27	negative voltage reference level input for the DACs
I_{ref}	28	current reference output
V_{DACP}	29	positive voltage reference level input for the DACs
BAIL	30	input of left channel buffer operational amplifier ‘A’
BAOL	31	output of left channel buffer operational amplifier ‘A’
NINL	32	negative input to left channel Sigma-Delta modulator
PINL	33	positive input to left channel Sigma-Delta modulator
BBOL	34	output of left channel buffer operational amplifier ‘B’
V_{refL}	35	voltage reference generator for the left channel analog section
V_{DDA}	36	supply voltage for the analog section (+5 V)
V_{SSA}	37	supply ground for the analog section

SYMBOL	PIN	DESCRIPTION
HPEN	38	high-pass filter enable input (HPEN = HIGH = enabled); if unconnected this pin defaults HIGH
TSEL	39	input to select master (TSEL = LOW) or slave (TSEL = HIGH) operation of the serial interface; if unconnected this pin defaults HIGH
WSEL	40	input to indicate 16-bit (WSEL = HIGH) or 18-bit (WSEL = LOW) output data word length of the serial interface; if unconnected this pin defaults HIGH
ODF2 and ODF1	41 and 42	serial interface format inputs; these 2 pins determine the interface format in which the device will operate (see Chapter “Functional Description”); if unconnected these pins will default HIGH (I^2S format)
$\overline{\text{RESET}}$	43	Power-On Reset (POR) input (active LOW) to mute the digital output during power on
CEN	44	Chip enable input; this pin, when LOW, disables the operation of the device and 3-states the outputs of the serial interface bus. This enables the connection of one of more devices to the output bus; if unconnected this pin defaults HIGH.

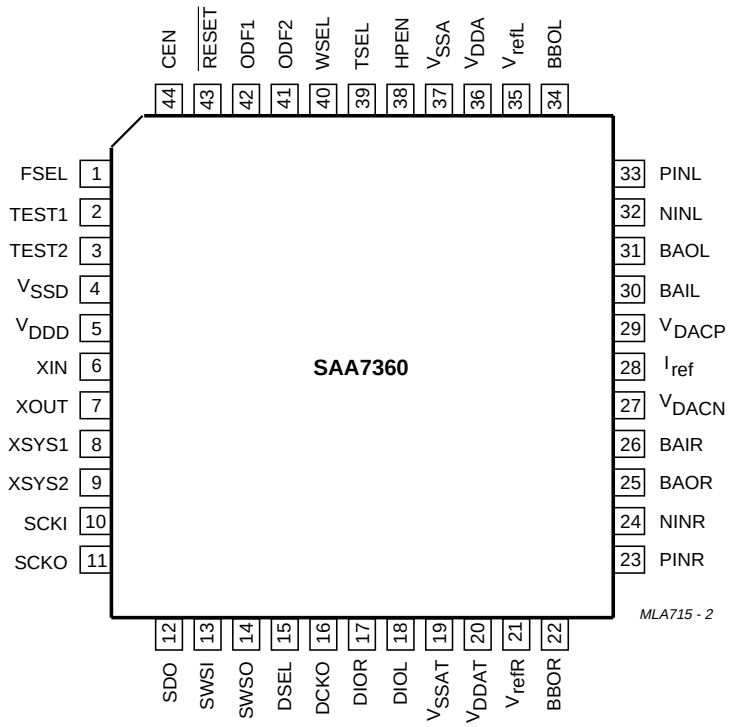


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The SAA7360 is a bitstream conversion CMOS ADC for digital audio systems. The device consists of a input buffer which can be configured by the user for pre-scaling and anti-aliasing, a third order Sigma- Delta modulator with a performance of better than 90 dB THD + Noise, and decimation filters with anti-aliasing suppression of >93 dB and in band ripple of less than 0.0002 dB. The device outputs data in a number of formats compatible with a range of manufacturers.

Clock frequency

The SAA7360 can operate in either master or slave mode (CMOS input drive levels). The clock can be either $256f_s$ or $512f_s$ (where f_s is the sampling frequency) indicated via pin FSEL. System clock outputs equal to the input frequency (XSYS1) and half the input frequency (XSYS2) are provided to drive other ICs in the system. All performance parameters track with f_s which can vary between 18 and 53 kHz without degradation of performance.

Input buffer

The input buffer stage consists of an uncommitted input operational amplifier (‘A’) and a committed unity gain operational amplifier (‘B’) to perform a single-to-double ended conversion for the differential ADC. The input buffer can be configured for pre-scaling and second order anti-aliasing filtering. The scaling should be performed so as to provide a maximum of 1 V RMS value at the output of the operational amplifier.

Sigma-Delta modulator

The analog-to-digital conversion is performed by a third order Sigma-Delta modulator, which outputs a 1-bit code at $128f_s$ with a distortion plus noise figure of >90 dB. The modulator is scaled so that a 0 dB input results in an output of −3 dB, at the 1-bit outputs.

Digital decimation filter

The left and right channel 1-bit codes from the ADC are decimated from $128f_s$ to $1f_s$ in four stages of filtering. The first filter stage decimates by a factor of $16f_s$ to $8f_s$ using a 4th order combination type filter. The other three filter stages consist of three cascaded half-band filters each decimating by a factor of two. The half-band filter decimating from $8f_s$ to $4f_s$ has a gain of +2 dB to compensate for the −3 dB through the analog part and allow a headroom of 1 dB to prevent clipping with DC offsets.

The overall response of the digital decimation filter is a pass band from $0f_s$ to $0.454f_s$ (20 kHz at f_s = 44.1 kHz) with a ripple of <0.0002 dB and a transition band of $0.454f_s$ to $0.544f_s$. All frequencies between $0.544f_s$ and $64f_s$ which could result in aliasing into the base band are attenuated by >−93 dB.

High-pass filter

The operational amplifiers in the Sigma-Delta modulator can cause a small DC offset to be present in the 1-bit code passed to the digital section. This can result in the possibility of clicks when switching between devices and the recording of DC offsets which can upset offsets introduced in filters and noise shaping DACs in the playback path. A switchable high-pass filter is included on the IC after the decimation filter stage to allow the user to remove these DC offsets (selectable via pin HPEN). The filter does not affect the decimation process. The filter is 1st order high pass with following specifications:

- Corner frequency (−3 dB): 1.7 Hz
- Ripple: none
- Above 100 Hz: <0.00002 dB; <1 degree
- At 20 Hz: −0.03 dB, 5 degree phase deviation
- Noise floor: −116 dB.

Output interface

The output interface can operate in master or slave mode selectable by pin TSEL. Master mode drives pins SWSO (word select), SCKO (bit clock) and SDO (data output). Slave mode receives the word clock on pin SWSI and the bit clock on pin SCKI. In slave mode the internal circuitry runs on the incoming bit clock and therefore cannot operate with burst clocks. Slave mode causes the pins SWSO and SCKO to be 3-stated allowing systems to connect SWSO and SCKO to pins SWSI and SCKI respectively for applications where the device has to operate in master and slave modes. The bit clock in master mode is at $32f_s$ for 16-bit output, and $64f_s$ for 18-bit output. In slave mode the bit clock is a minimum of $32f_s$ and a maximum of $64f_s$.

Three output formats are supported, I^2S and two pseudo I^2S modes common in digital audio ADC systems. These formats are shown in Fig.3. Selection of the three formats is given in Table 1. 16-bit or 18-bit output words can be chosen (via pin WSEL).

Table 1 Output data formats

ODF2	ODF1	MODE
0	0	test
0	1	format 1
1	0	format 2
1	1	I^2S

Reset

When pin $\overline{\text{RESET}}$ is held LOW the data outputs are set to zero. The $\overline{\text{RESET}}$ pin operates as a Schmitt trigger, enabling a power-on reset function by using an external RC circuit.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage	note 1	–0.5	+6.5	V
V_I	DC input voltage		–0.5	+6.5	V
I_{IK}	DC input diode current		–	±20	mA
V_O	DC output voltage		–0.5	V_{DD} + 0.5	V
I_O	DC output source or sink current		–	±20	mA
I_{DD} or I_{SS}	total DC V_{DD} or V_{SS} current		–	±0.5	A
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–65	+150	°C
V_{es}	electrostatic handling	note 2	–2000	+2000	V
		note 3	–200	+200	V

Notes

1. All V_{DD} and V_{SS} pins must be externally connected to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor with a rise time of 15 ns.
3. Equivalent to discharging a 200 pF capacitor via a 2.5 μH series inductor.

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; $f_{xtal} = 256f_s$; f_s = 44.1 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		4.5	5.0	5.5	V
I_{DDA}	analog supply current		–	43	–	mA
V_{DDD}	digital supply voltage		4.5	5.0	5.5	V
I_{DDD}	digital supply current		–	50	–	mA
P_{tot}	total power consumption		–	465	–	mW

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital part inputs						
FSEL, HPEN, DSEL, TSEL, WSEL, ODF2, ODF1 AND CEN						
V_{IL}	LOW level input voltage	note 1	–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
Z_i	input impedance		–	35	–	kΩ
C_i	input capacitance		–	–	10	pF
$\overline{\text{RESET}}$						
V_{IL}	LOW level input voltage	note 1	–0.5	–	+0.2V_{DDD}	V
V_{IH}	HIGH level input voltage	note 1	0.6V_{DDD}	–	V_{DDD} + 0.5	V
ΔV_I	input hysteresis		0.2	–	–	V
I_{LI}	input leakage current	note 2	–10	–	+10	μA
C_i	input capacitance		–	–	10	pF
SCKI and SWSI						
V_{IL}	LOW level input voltage	note 1	–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current		–10	–	+10	μA
C_i	input capacitance		–	–	10	pF
Crystal oscillator input XIN						
V_{IL}	LOW level input voltage		–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage		0.7V_{DDD}	–	V_{DDD} + 0.5	V
I_{LI}	input leakage current	note 2	–10	–	+10	μA
C_i	input capacitance		–	–	10	pF
Outputs						
SWSO, SCKO AND SDO						
V_{OL}	LOW level output voltage	–400 μA; note 1	–	–	+0.4	V
V_{OH}	HIGH level output voltage	20 μA; note 1	2.4	–	–	V
C_L	load capacitance		–	–	50	pF
I_{LI}	leakage current in 3-state	note 2	–10	–	+10	μA
XSYS1 AND XSYS2						
V_{OL}	LOW level output voltage	–400 μA; note 1	–	–	0.4	V
V_{OH}	HIGH level output voltage	20 μA; note 1	2.4	–	–	V
C_L	load capacitance		–	–	35	pF
DCKO						
V_{OL}	LOW level output voltage	–400 μA; note 1	–	–	1.0	V
V_{OH}	HIGH level output voltage	20 μA; note 1	V_{DDD} – 1.0	–	–	V
C_L	load capacitance		–	–	20	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input/outputs DIOR and DIOL						
V_{IL}	LOW level input voltage	note 1	–0.5	–	+0.8	V
V_{IH}	HIGH level input voltage	note 1	2.0	–	V_{DDD} + 0.5	V
Z_i	input impedance		–	35	–	kΩ
C_i	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	–400 μA; note 1	–	–	1.0	V
V_{OH}	HIGH level output voltage	20 μA; note 1	V_{DDD} – 1.0	–	–	V
C_L	load capacitance		–	–	20	pF
Crystal oscillator input XIN and output XOUT						
f_{xtal}	crystal operating frequency	note 3	4.608	$256f_s$ or $512f_s$	27.136	MHz
G_m	mutual conductance	100 kHz	1.5	–	–	mA/V
G_v	small signal voltage gain	$G_v = G_m \times R_o$	–	3.5	–	V/V
C_i	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
C_o	output capacitance		–	–	10	pF
I_{LI}	input leakage current	note 2	–10	–	+10	μA
Timing						
External clock input XIN						
f_i	input frequency	note 3	4.608	$256f_s$ or $512f_s$	27.136	MHz
t_r	input rise time	V_{IL} to V_{IH}	–	–	10	ns
t_f	input fall time	V_{IH} to V_{IL}	–	–	10	ns
msr	mark-space ratio	slave mode; $256f_s$	45	–	55	%
		slave mode; $512f_s$	40	–	60	%
System clock outputs XSYS1 and XSYS2 (note 4)						
t_r	output rise time	V_{OL} to V_{OH}	–	–	15	ns
t_f	output fall time	V_{OH} to V_{OL}	–	–	15	ns
t_H	output HIGH time (relative to clock period)	note 5	40	50	60	%
1-bit code outputs (see Fig.4)**; 1–bit code inputs** (see Fig.5)						
CLOCK DCKO						
t_r	clock output rise time	note 6	–	–	15	ns
t_f	clock output fall time	note 6	–	–	15	ns
t_H	clock output HIGH time		45	–	–	ns
t_L	clock output LOW time		45	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DATA DIOL AND DIOR						
t_{dor}	data output rise time	note 6	–	–	15	ns
t_{dof}	clock output fall time	note 6	–	–	15	ns
t_d	data output delay time (relative to DCKO)	note 6	–30	–	+30	ns
t_{dir}	data input rise time		–	–	20	ns
t_{dif}	data input fall time		–	–	20	ns
t_{su}	data input set-up time (relative to DCKO)		30	–	–	ns
t_h	data input hold time (relative to DCKO)		30	–	–	ns
Serial data outputs (see Fig.6)						
CLOCK SCKO						
t_r	clock output rise time	note 7	–	–	30	ns
t_f	clock output fall time	note 7	–	–	30	ns
WORD SELECT SWSO						
t_r	word select output rise time	note 7	–	–	30	ns
t_f	word select output fall time	note 7	–	–	30	ns
t_{sr}	word select output set-up time	note 8	100	–	–	ns
t_{hr}	word select output hold time	note 8	100	–	–	ns
CLOCK SCKI (note 9)						
t_r	clock input rise time		–	–	100	ns
t_f	clock input fall time		–	–	100	ns
t_{HC}	clock input HIGH time		50	–	–	ns
t_{LC}	clock input LOW time		50	–	–	ns
WORD SELECT SWSI (note 9)						
t_r	word select input rise time		–	–	100	ns
t_f	word select input fall time		–	–	100	ns
t_{sr}	word select input set-up time	note 10	100	–	–	ns
t_{hr}	word select input hold time	note 10	100	–	–	ns
DATA SDO						
t_r	data output rise time	note 7	–	–	30	ns
t_f	data output fall time	note 7	–	–	30	ns
t_{dod}	data output delay time	note 10	–100	–	+100	ns
t_{sr}	data output set-up time	note 8	100	–	–	ns
t_{hr}	data output hold time	note 8	100	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part						
VOLTAGE REFERENCE V_{refL} AND V_{refR}						
V_I	input voltage		2.0	2.3	2.7	V
Current reference I_{ref} (note 11)						
I_O	output current		–	$\frac{V_{refR}}{13\ k\Omega}$	–	A
DAC reference						
INPUT V_{DACN}						
V_I	input voltage		–	V_{SSA}	–	V
INPUT V_{DACP}						
V_I	input voltage		–	V_{DDA}	–	V
Sigma-Delta modulator inputs PINR, NINR, PINL and NINL						
$V_{I(rms)}$	input voltage (RMS value)	note 12	–	1	–	V
ADC performance (note 13)						
THD + N	total harmonic distortion + noise	at –1 dB digital output; note 14	–	–90 (0.003%)	–85 (0.0056%)	dB
DR	dynamic range	note 14	93	97	–	dB
α_{cs}	channel separation	f_i = 1 kHz; note 15	–	100	–	dB
G	gain		–1.5	–1	–0.5	dB
t_{gd}	group delay (in pass band)	note 16	–	1.25	–	ms

Notes

1. Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
2. I_{LI} minimum and I_{LO} minimum measured at V_I = 0 V; I_{LI} maximum and I_{LO} maximum measured at $V_I = V_{DDD}$.
3. f_{xtal} is a multiple of the system sampling frequency f_s which can vary between 18 and 53 kHz.
4. Output times are measured with a capacitive load of 35 pF; XSYS2 is the master clock frequency divided by 2.
5. t_H valid only when used with XTAL, with 50% input mark space ratio; XSYS1 (t_H) is measured at $\frac{1}{2}V_{DDD}$.
6. Output times are measured with a capacitive load of 20 pF.
7. Output times are measured with a capacitive load of 50 pF.
8. Relative to SCKO in master mode.
9. In slave mode the number of SCKI clocks in each channel should be <33 and the same in both. The polarity of SWSI indicates left/right channel.
10. Relative to SCKI in slave mode.
11. I_{ref} connected to 0 V via a 13 kΩ resistor.
12. The maximum recommended input voltage (referred to as 0 dB) yields a –1 dB output (relative to full-scale digital swing). The input voltage scales with $V(V_{DACP}) - V(V_{DACN})$; almost equal to V_{DDA}, hence:

$$V_I\ (0\ dB) = \frac{[V(V_{DACP}) - V(V_{DACN})]}{5} V\ (RMS\ value)$$

13. Device measured with external components as shown in recommended application diagram (see Fig.7).

14. Typical values are for 18-bit performance, minimum and/or maximum values are for 16-bit performance.
15. This is the ratio (in dB) of the digital output amplitude of single tone, in one channel, to the digital output amplitude of the same tone in the measurement channel. This definition presupposes that the channels have the same gain.
16. Group delay $= \frac{(55.5 \pm 1)}{f_s}$, where f_s is the output sampling frequency. Typical value given is for f_s = 44.1 kHz.

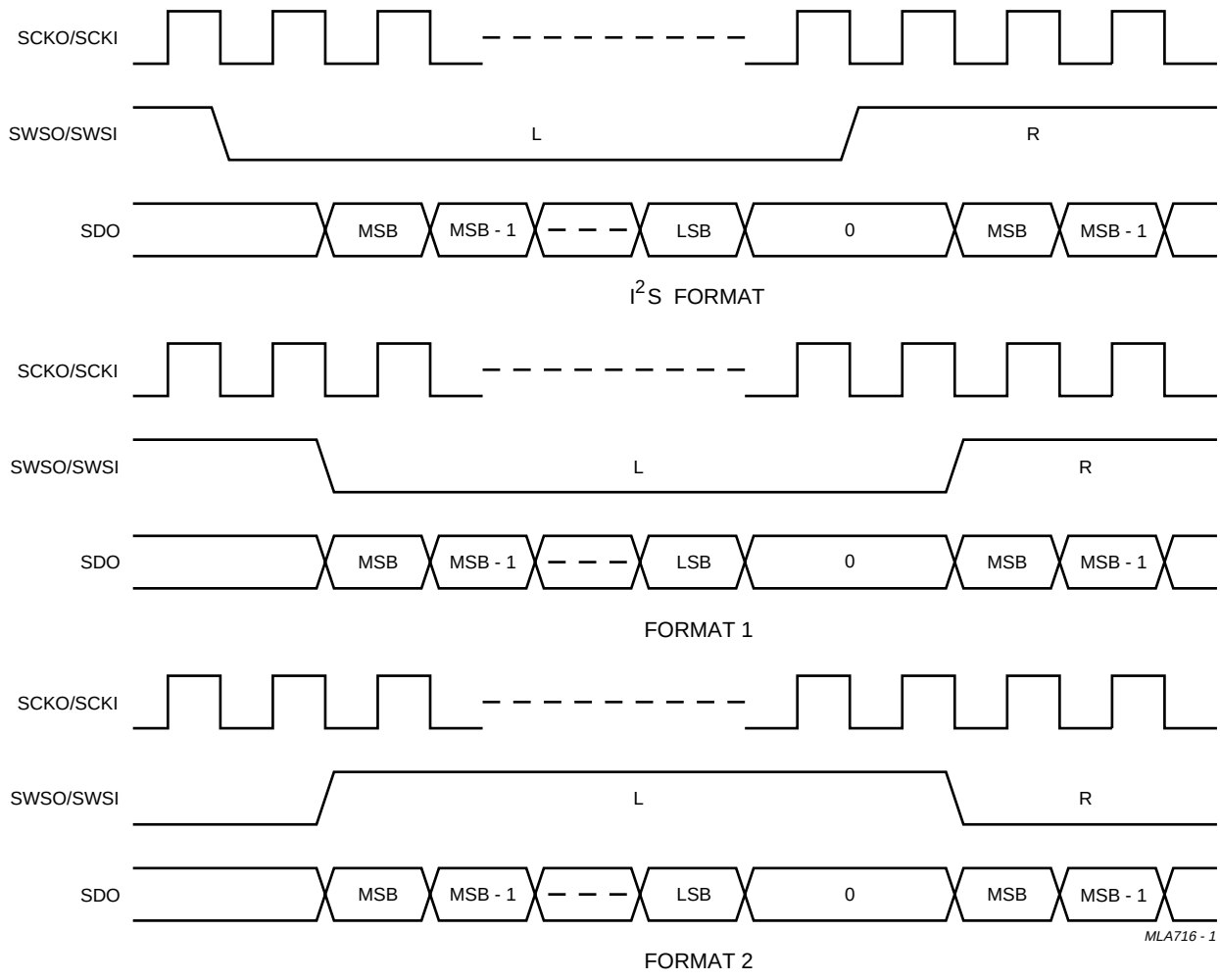


Fig.3 Output interface modes.

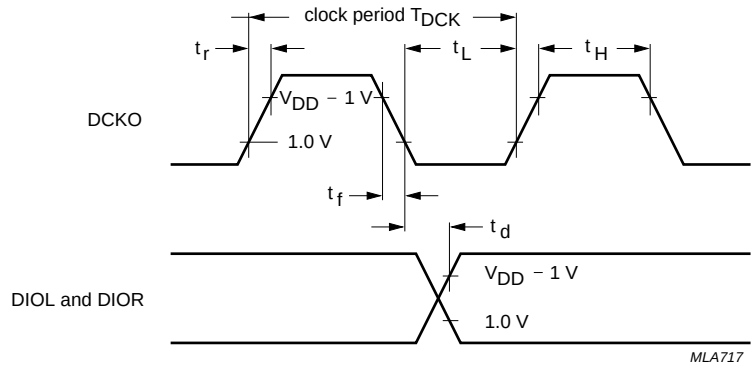


Fig.4 One bit code output timing.

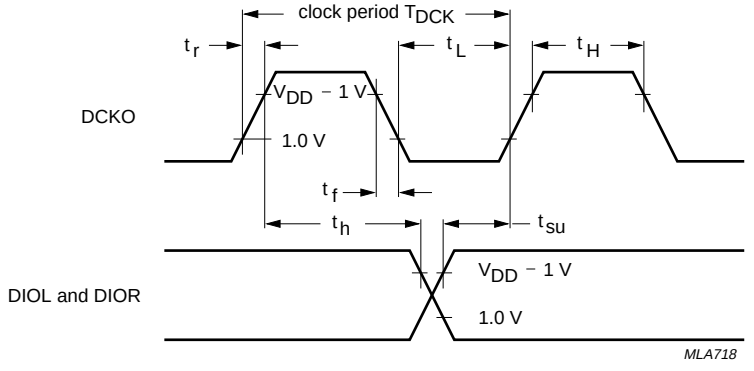


Fig.5 One bit code input timing.

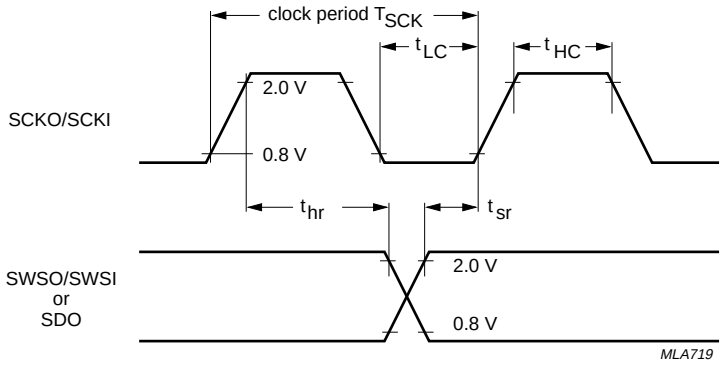


Fig.6 Serial output timing.

APPLICATION INFORMATION

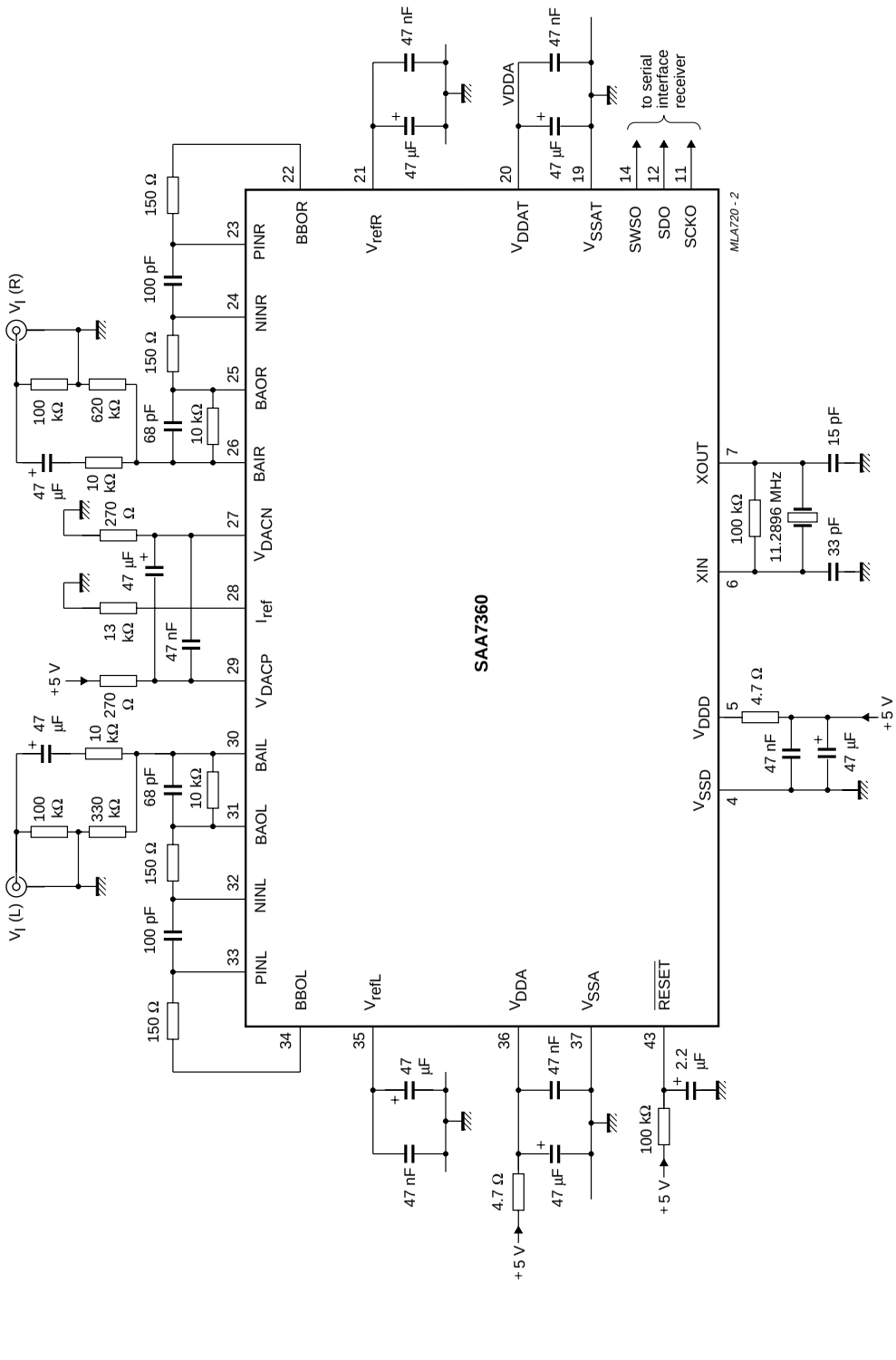
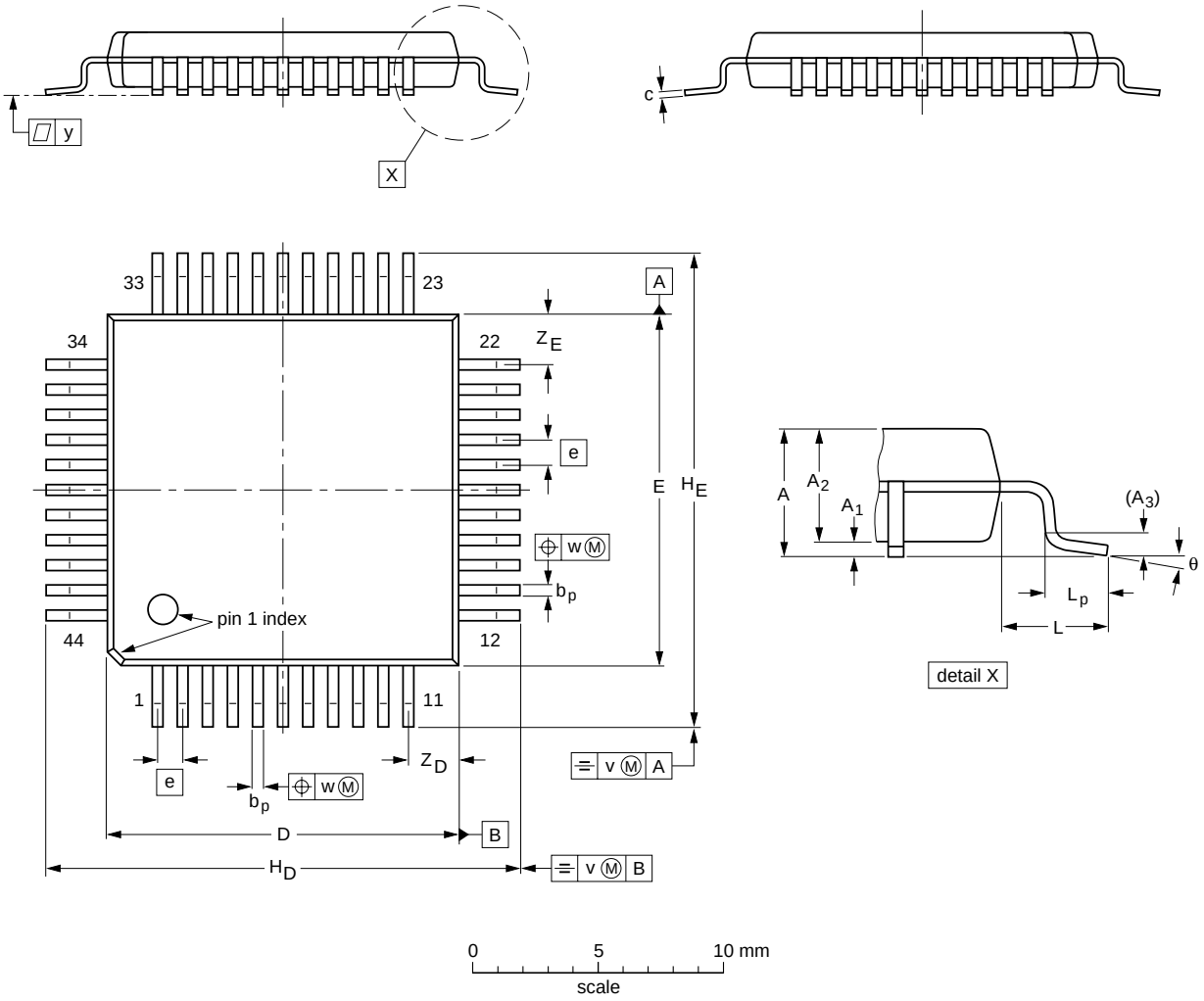


Fig.7 Application diagram.

Pins 1 to 3, 8 to 10, 13, 15 to 18, 38 to 42 and 44 are not connected.

PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~95-02-04~~ 97-08-01

SOLDERING

Plastic quad flat packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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